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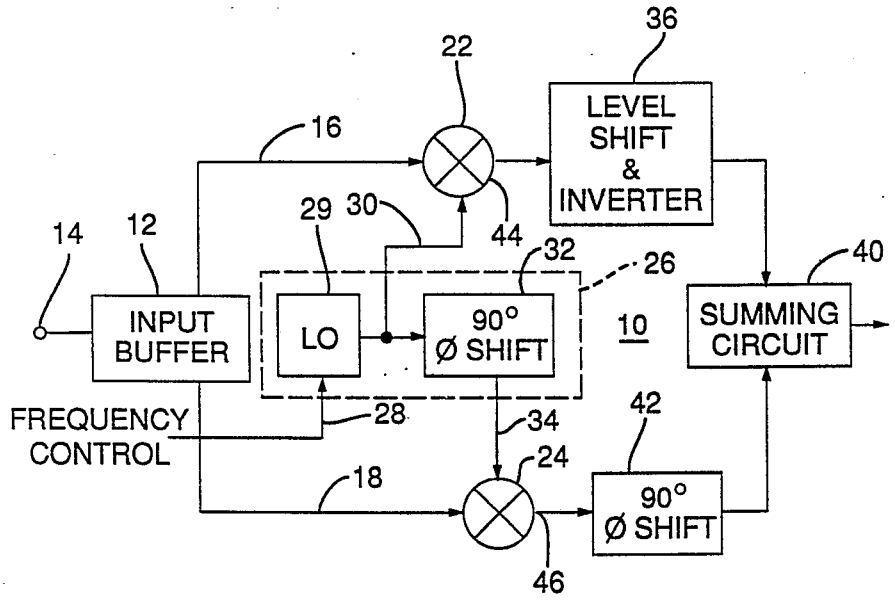

(57) Abstract

An IF mixer circuit (10) in a receiver implemented in integrated circuits employs a pair of doubly balance mixers (22, 46), one injected with a local oscillator reference signal in phase while the quadrature phase of the reference signal is injected into the second mixer. A phase shift circuit (42) adds another 90° phase shift to the output of the second mixer (46), and the in-phase and out-of-phase signals are applied to a summing circuit (40) to attenuate unwanted mixer products and reinforce the desired IF signal. The balanced elements of the 90° phase shift circuit (42) employ a transistor (61) with equal emitter and collector resistances, a diode-connected transistor (63) in series with the collector load resistance (65), and a collector-to-base capacitor (67), which provide a constant-amplitude phase shift in a unity gain structure independent of current, to produce a precise 90° phase shift. Emitter current is adjustable to compensate for production variation in the absolute value of the fixed resistance, i.e., by varying the current in the transistor and diode, the dynamic resistance offsets the fixed resistance variation.

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IMAGE CANCELING MIXER CIRCUIT ON AN INTEGRATED CIRCUIT CHIP

Field of the Invention

This invention relates generally to telecommunications and particularly to an integrated circuit frequency conversion circuit.

Background of the Invention

Copending patent application serial number 07/213,719 filed June 30, 1988 by Lawrence H. Ragan and entitled Wristwatch Receiver Architecture describes an FM radio receiver suitable for paging applications, and constructed on a single integrated circuit chip having only a small number of off-chip components. It is desirable to minimize the number of discrete, off-chip components because it reduces the cost of the unit, provides additional space in the package formerly occupied by the discrete components, and makes the device less labor-intensive to assemble.

A mixer circuit in a receiver translates a signal received at one frequency to another frequency, termed an intermediate frequency (IF), at which the signal can be processed more conveniently and effectively. The intermediate frequency facilitates processing, filtering and detecting a signal with greater ease and efficiency than would be possible were the signal kept at the radio

frequency at which it was transmitted and propagated. A problem inherent in all mixer circuits is generation of image frequency signals. When two signals are mixed, signal components are produced at the sum and difference of the two signal frequencies and at the harmonics of the frequencies. It is desirable to reduce or eliminate the image-frequency response of the mixer circuit, however it is often impractical to filter out the image frequency. Post-mixer filtering has been found to be inadequate because input signal images can be mixed to the same intermediate frequency as the desired signal. Image-rejection mixer circuits utilizing phase-shifting techniques are known, however such circuits have heretofore used transmission lines, operational amplifiers or L-C networks, none of which are conducive to implementation in a single-chip integrated circuit receiver.

Summary of the Invention

According to the present invention, a single-chip integrated circuit radio receiver, which is designed for use in a radio paging system, includes an improved on-chip image-rejection mixer circuit. An amplified, wide-band RF input signal is split and applied to inputs of first and second doubly balanced mixers, while a local oscillator signal is injected into the first mixer in phase, and shifted in phase by 90° into the second mixer. The quadrature outputs of the second mixer are applied to

a balanced phase shift element where the signals are shifted an additional 90°, and then combined with the outputs of the in-phase mixer, the summation of these signals canceling the image frequency while reinforcing the desired signal.

The balanced 90° phase shift element employs transistors each having a diode-connected transistor in series with the collector load resistor, and a collector-to-base capacitor, which provide a constant-amplitude phase shift in a unity gain structure independent of current, with equal emitter and collector resistances. Emitter current is adjustable to produce a precise 90° phase shift. The adjustment compensates for production variation in the absolute value of the fixed resistance by varying the current in the transistor and diode, whereby the dynamic resistance offsets the fixed resistance variation. The improved mixer circuit has a conversion gain at the desired signal frequency of approximately 7 dB.

Brief Description of the Drawing

While the invention is set forth with particularity in the appended claims, other objects, features, the organization and method of operation of the invention will become more apparent, and the invention will best be understood by referring to the following detailed description in conjunction with the accompanying drawing in which:

FIG. 1 is a block diagram of an improved image-rejecting mixer circuit in accordance with the instant invention;

FIGS. 2 and 3, taken together, are a schematic diagram of the circuit of FIG. 1; and

FIG. 4 is an idealized representation of the 90° phase shift circuit of FIG. 2.

Description of the Preferred Embodiment

Referring now to the various views of the drawing for a more detailed description of the components, materials, construction, function, operation and other features of the instant invention by characters of reference, FIG. 1 shows an image-rejecting mixer circuit 10 having an input buffer 12 receiving an amplified, broad-band radio frequency (RF) signal, suitably in the FM broadcast band, 88-108 megahertz, on an input node 14 from a receiver RF stage (not shown). The buffered RF signal, split in a conventional manner, is applied respectively by way of buses 16, 18 to the low-level signal inputs of doubly-balanced mixers 22, 24. A frequency synthesizer 26, assuming high-side injection, tunes the 98.7 to 118.7 megahertz range in response to frequency control signal 28 to yield an IF of 10.7 megahertz. A local-oscillator (LO) 29 operating in the 240 megahertz range generates an in-phase signal from a conventional divide-by-two frequency divider circuit (not shown), which is applied via bus 30 to the high-level signal input of the mixer

22. The phase of the LO signal is shifted 90° in phase-shift circuit 32 and applied by way of bus 34 to the high-level input of the mixer 24. A precise 90° phase shift is obtained by utilizing the quadrature output logically derived from an exclusive OR of the fundamental output of the local oscillator 29 and the divide-by-two frequency divider circuit. The output signals of the in-phase mixer 22 are applied through a level shift and inverter circuit 36 to a summing circuit 40, while the output signals of the 90° mixer 24 are applied to a phase shift circuit 42, where they are inverted and shifted in phase an additional 90°, then applied to the summing circuit 40. Phase difference of the signals is preserved in the frequency transformation of the mixers 22, 24, so that the IF components output have the same phase relationships as the original LO input terms, i.e., the signals output from the in-phase mixer 22 at node 44 undergo no phase shift and are downconverted in the conventional manner, while the signals output from the 90° mixer 24 at node 46 undergo a 90° delay relative to those at the node 44.

Referring to FIGS. 2 and 3, the circuit of FIG. 1 is shown in greater detail. The input buffer 12 and the in-phase mixer 22, which is a conventional integrated circuit doubly balanced mixer, receives the low-level RF signals from the input buffers 12 into the bases of transistors 50, 51, the high-level, in-phase LO signals

being injected into the bases of transistors 52-55. Mixer 22 output signals I_1, I_2 and mixer 24 output signals D_1, D_2 are applied to level shifting circuits 58, which are emitter-follower transistors. Current regulating transistors 60 provide impedance matching between the mixers 22, 24, and the respective circuits 36, 42.

Phase shifter circuit 42 comprises two balanced circuits receiving the balanced output signals D_1, D_2 from the mixer 24 and input respectively to the bases of transistors 61, 62. The collectors of transistors 61, 62 are connected through respective diode-connected transistors 63, 64 and 500 ohm emitter resistors 65, 66 to voltage supply V_{cc}. Balanced MOS capacitors 67, 68 are connected respectively between the emitter and base of transistors 61, 62, and 500 ohm resistors 69, 70 are connected respectively between the emitters of transistors 61, 62 and the collector of a current-source transistor 71. The circuit 42 provides an all-pass filter transfer function for the differential voltage between base nodes 72, 73 to the output differential voltage at output nodes 74, 75. The circuit 42 has a nominal unity gain transfer function with a phase shift equal to $-2 \arctan (R'C)$, where R' is $R + (KT/I_cq)$, and I_c is quiescent collector current. The derivation is as follows: Referring to FIG. 4, an idealized representation of the 90° phase shift circuit 42 is shown, wherein beta ■

and transconductance gm are assumed to be infinity ∞. It is seen that for AC quantities:

$$I_R := V_E/R$$

and

$$V_o := (I_{cap} - I_R) \blacksquare R$$

Substituting

$$V_o := (I_{cap} - V_E/R) \blacksquare R$$

$$V_{in} := V_E$$

$$V_o := I_{cap} \blacksquare R - V_{in}$$

$V_o := (V_{in} - V_o) \blacksquare C \blacksquare S \blacksquare R - V_{in}$, where C■S is admittance;

$$V_o := V_{in} \blacksquare [(-1 + R \blacksquare C \blacksquare S)/(1 + R \blacksquare C \blacksquare S)]$$

$$V_o := -[(1 - R \blacksquare C \blacksquare S)/(1 + R \blacksquare C \blacksquare S)] \blacksquare V_{in}$$

The above is a one-pole, all pass filter function.

The function of diode-connected transistors 63, 64 is to achieve a collector load resistance equal to the emitter resistance plus dynamic emitter resistance, thereby obtaining a unity gain characteristic. The dynamic resistance term KT/I_cq facilitates adjustment of the total resistance and the R'C time constant to a value which will produce a 90° phase shift at a frequency $f = 1/(R'C)$. The emitter current is variable by way of an external resistor 76 connected to a bonding pad 77 of the integrated circuit chip. The emitter current source transistor 71 mirrors a circuit 78 which is a proportional-to-absolute-temperature (PTAT) bias current source; therefore, the incremental resistance of the

diodes 63, 64 is maintained over a temperature range, providing a stable resistance and time constant as a function of temperature. Since the collector load tracks the emitter load as current is varied, unity gain is preserved and only the phase is varied.

The level shift and inverter circuit 36 provides a gain block for the in-phase signals I_1, I_2 of mixer 22 input respectively by way of output nodes 79, 80 of the level shifting circuit 58. The circuit 36 adjusts for losses in the signal path. The summing circuit 40 sums the in-phase signals from nodes 81, 82 and the out-of-phase signals from nodes 74, 75, injected, respectively, into the bases of transistors 84-87, the summation occurring at nodes 90, 92 where the collector currents, respectively, of transistors 84, 86 and 85, 87 are added together. Output signals at the nodes 90, 92 are driven into the bases, respectively, of balancing transistor 94 and output transistor 95 of output circuit 96, which provides an output signal at a node 98 to a single ended filter stage (not shown).

The delay of the D_2 signal output from node 99 of the mixer 24 is manifest by a negative 90° phase shift in the positive frequency components and a positive 90° phase shift in the negative frequency components. When the D_2 signal is then subjected to the additional 90° delay of the circuit 42 at node 69, the IF components from the

upper sideband terms have been shifted 180° and the lower sideband terms again remain unchanged. When the D_2 and I_2 signals are summed at node 92 in the summing circuit 40, the upper sideband components cancel and the unshifted lower sideband terms remain. By the same rationale, the other output at the node 90 contains the desired upper sideband terms of the IF signal.

The mixer circuit thus, by virtue of its symmetry and internal balance, reinforces the desired signal and suppresses and substantially attenuates harmonic and image frequency products. Efficient phase cancellation is achieved through the ability to maintain extremely accurate phase angles. The initial 90° phase shift is derived digitally in a frequency synthesizer circuit, while the phase shift circuit 42 provides a constant-amplitude phase shift in a unity gain structure independent of current, with equal emitter and collector resistances, the emitter current being adjustable to produce the second, precise 90° phase shift. The adjustment compensates for production variation in the absolute value of the fixed resistance by varying the current in the transistors 61, 62 and diodes 63, 64, whereby the dynamic resistance offsets production variation of the fixed resistance.

While the principles of the invention have now been made clear in the foregoing illustrative embodiment, there will be immediately obvious to those skilled in the art many modifications of structure, arrangement, proportions, the elements, material and components used in the practice of the invention, and otherwise, which are particularly adapted for specific environments and operating requirements without departing from those principles. The appended claims are, therefore, intended to cover and embrace any such modifications, within the limits only of the true spirit and scope of the invention.

Claims

1. An image-rejecting mixer circuit on an integrated circuit chip, comprising: first and second mixers each receiving a radio frequency signal, the first mixer receiving a local-oscillator reference signal, the second mixer receiving the local-oscillator reference signal shifted in phase by 90°;

a phase-shift circuit coupled to the second mixer and receiving the converted product signals therefrom, the phase-shift circuit delaying the converted product signals an additional 90° and including means for adjusting the phase angle of the signal output therefrom; and

a summing circuit coupled to the first mixer and the 90° phase-shift circuit, the summing circuit combining in-phase components of converted product signals from the first mixer with the converted product signals of the second mixer delayed by 180°, whereby the image frequency components of the combined signals are substantially attenuated.

2. The mixer circuit of claim 1 wherein the phase-shift circuit comprises a unity gain transistor amplifier having a base circuit receiving the converted product signals from the second mixer, a collector to base capacitor, an emitter load including a fixed resistor, and a collector load including a fixed resistor in series with a diode-connected transistor, the adjusting means including an adjustable emitter load resistor, whereby a variation in emitter load current introduced by the adjustable resistor varies dynamic emitter resistance to compensate for production variations of the fixed resistors and produces an RC time constant which results in a 90° phase shift of the output signal.

3. The mixer circuit of claim 2 further comprising a temperature compensating current source in the adjustable emitter load of the phase-shift circuit.

4. An integrated-circuit phase shift element comprising: a unity gain amplifier circuit having an NPN transistor with a base receiving an input signal, a collector to base capacitor, an emitter load including a fixed resistor, and a collector load including a fixed resistor in series with a diode-connected transistor, the amplifier circuit having means for adjusting the phase angle of an output signal with respect to the input signal, the phase shift adjusting means including an adjustable emitter load resistor, whereby a variation in emitter load current introduced by the adjustable resistor varies dynamic emitter resistance to compensate for production variations of the fixed resistors and produces an RC time constant which results in a desired phase shift of the output signal with respect to the input signal, wherein collector load current tracks the varying emitter load current to preserve the unity gain of the amplifier circuit as the phase is varied.

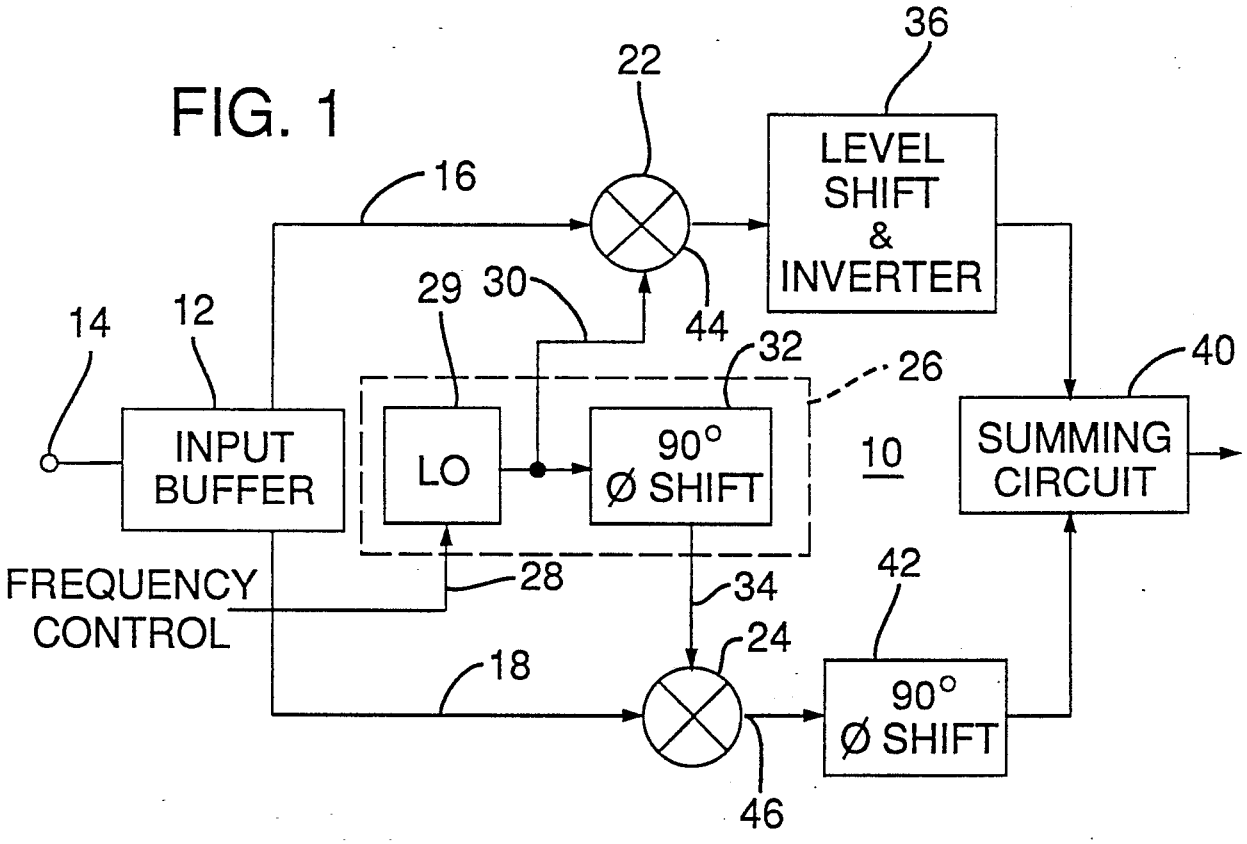
5. The integrated-circuit phase shift element of claim 4 further comprising a temperature compensating current source in the emitter load of the unity gain amplifier circuit.

6. An image canceling mixer circuit including means for generating a first in-phase reference frequency signal; means for generating a second reference frequency signal shifted in phase by 90° with respect to the first reference frequency signal; first means receiving a radio frequency input signal for mixing the input signal with the first reference frequency signal to generate an in-phase composite signal; second means receiving the radio frequency input signal for mixing the input signal with the second reference frequency signal to generate a quadrature composite signal; means coupled to the second mixing means for shifting the phase of the quadrature composite signal an additional 90° to generate a composite signal shifted in phase by 180° with respect to the in-phase composite signal; means for summing the in-phase composite signal and the 180° composite signal to generate an intermediate frequency signal output having attenuated image-frequency components, the improvement comprising:

the phase shifting means including a unity gain amplifier circuit having an NPN transistor with a base receiving the quadrature composite signal, a collector to base capacitor, an emitter load including a fixed resistor, and a collector load including a fixed resistor in series with a diode-connected transistor, the amplifier circuit having means for adjusting the phase angle of the phase shift adjusting means and including an adjustable emitter

load resistor, whereby a variation in the emitter load current introduced by the adjustable resistor varies dynamic emitter resistance to compensate for production variations of the fixed resistors and produces an RC time constant which results in a 90° phase shift of the output signal with respect to the input quadrature composite signal, the collector load current tracking the varying emitter load current to preserve the unity gain of the amplifier circuit as the phase is varied.

FIG. 1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22
LEVEL SHIFT & INVERTER
16
29
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44
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32
26
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INPUT BUFFER
LO
90° Ø SHIFT
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SUMMING CIRCUIT
FREQUENCY CONTROL
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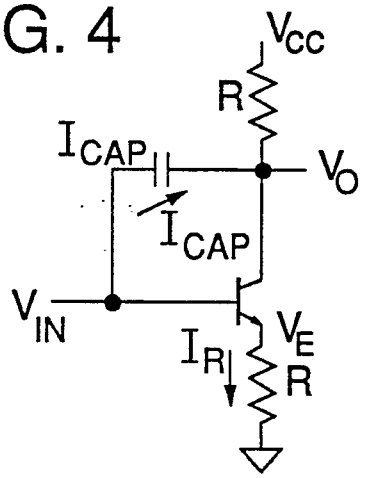
24
18
90° Ø SHIFT
46

FIG. 4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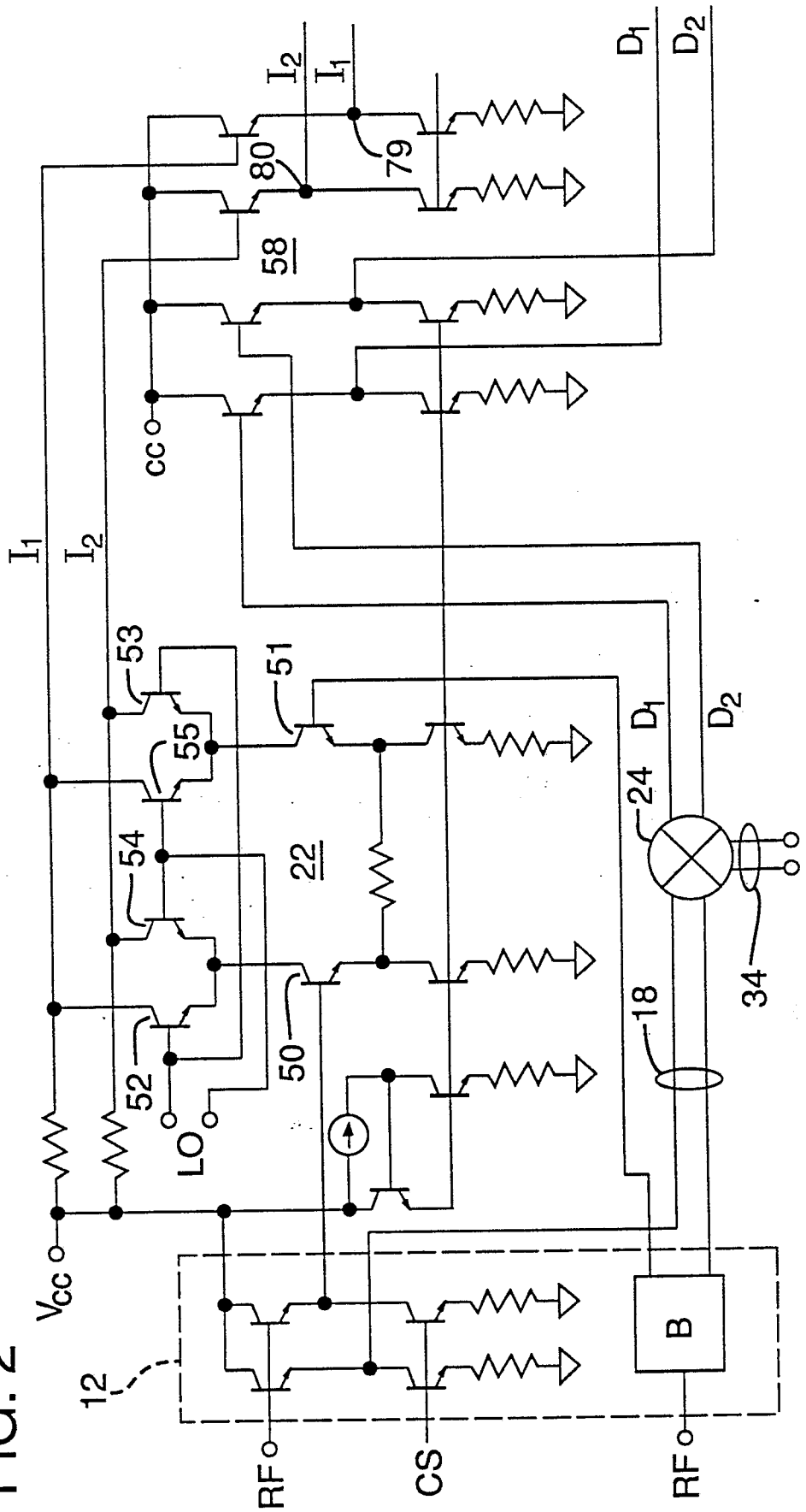
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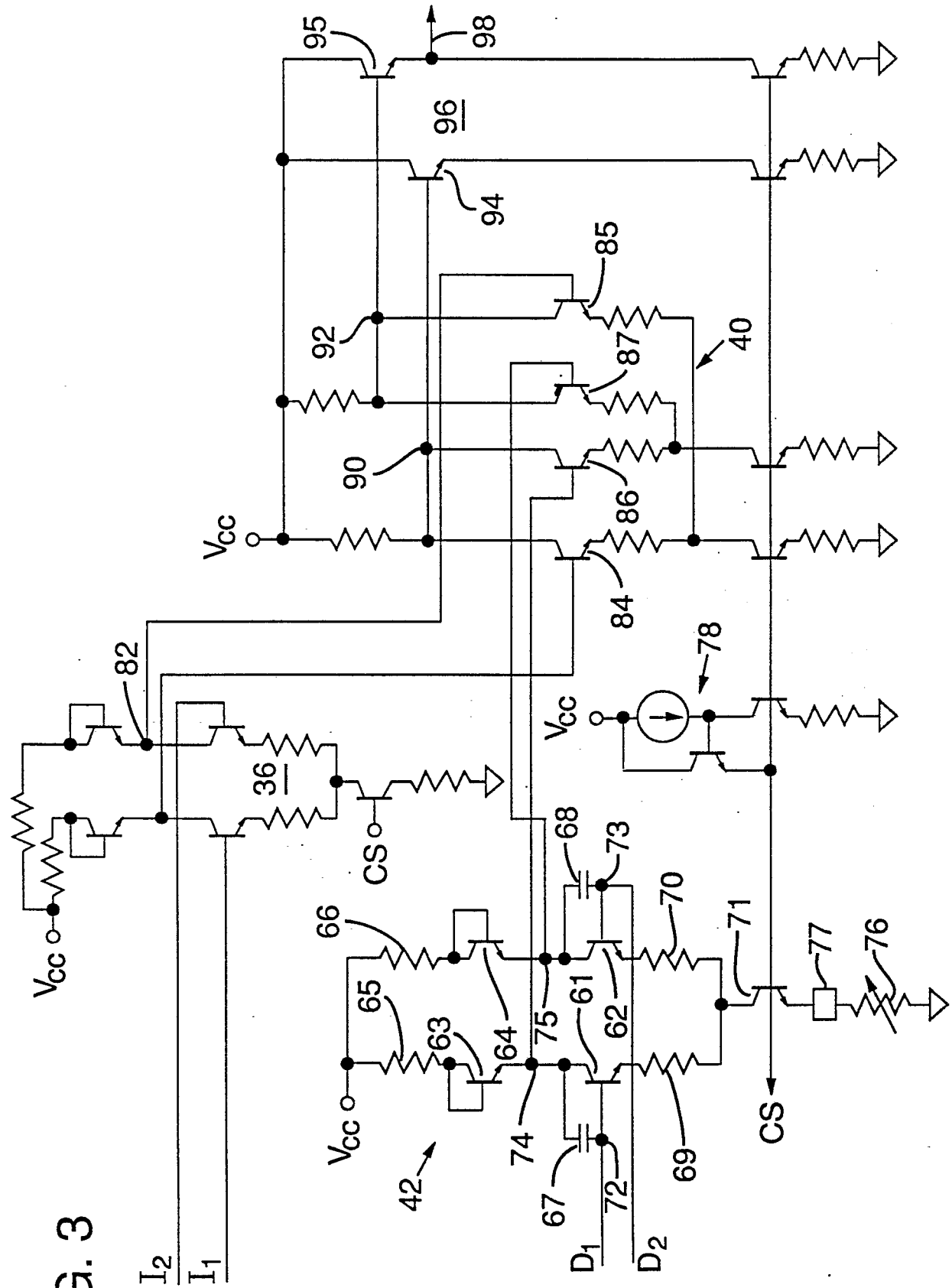
FIG. 2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D_1
D_2
I_2
I_1

FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No PCT/US90/04262

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5) : H04B 1/10; H03D 1/00
U.S. Cl : 307/520; 328/167; 455/302

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	307/491,262,520,521,529; 328/55,165,167,155; 455/302,303,304,305

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	US,A 4,710,814 (GASSMANN ET AL) 01 December 1987 See the entire document.	1
A	US,A 4,414,686 (LENZ) 08 November 1983	1-6
A	US,A 4,584,715 (BAARS ET AL) 22 April 1986	1-6
A	US,A 4,710,975 (OKAMOTO ET AL) 01 December 1987	1-6
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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
20 SEPTEMBER 1990	11 JAN 1991
International Searching Authority [1]	Signature of Authorized Officer [20]
ISA/US	TIMOTHY P. CALLAHAN